WHAT IS CLAIMED IS:

1. A method of designing an integrated circuit having digital and analog circuit portions, said digital and analog circuit portions each having defined functions, comprising:

providing an emulation circuit, which is capable of generating noise;

affixing said emulation circuit on a test substrate;

providing a version of said analog circuit portion having at least some of said defined functions of said analog circuit portion;

affixing said analog circuit version on said test substrate; and

testing said analog circuit version.

2. The method of claim 1 further comprising modifying said analog portion in response to said testing step.

3. The method of claim 2 further compromising:

repeating said affixing emulation circuit step, said analog circuit portion providing step, said analog circuit portion version affixing step and said analog circuit portion version testing circuit step so that a version of said analog circuit portion having all of said defined functions of said analog circuit portion, with acceptable response to said noise effects under operating conditions is obtained.

4. The method of claim 1 further comprising:

providing a version of said digital circuit portion having all of said defined functions of said digital circuit portion; and

affixing said digital circuit portion version to an integrated circuit including said version of said analog circuit portion having all of said defined functions of said analog circuit portion, with acceptable response to said noise effects under operating conditions.

5. The method of claim 4 wherein said digital circuit portion providing step includes testing said defined functions of said digital circuit portion separately from said analog circuit portion.

6. The method of claim 5 wherein said digital circuit portion testing includes programming an FPGA for testing said defined functions of said digital circuit portion.

7. The method of claim 5 wherein said digital circuit portion testing includes simulating said defined functions of said digital circuit portion.

8. The method of claim 1 wherein said emulation circuit comprises at least one array comprising at least one shift register.

9. The method of claim 8, wherein said testing said analog circuit version is performed while alternately shutting off and turning on at least one array.

10. The method of claim 8, wherein said shift register comprises:

a plurality of flip-flops, each having a clock input for receiving a clock input signal, and each storing a data bit; and

a plurality of interconnecting logic blocks, wherein said plurality of flip-flops couple to each other through said plurality of interconnecting logic blocks sequentially, and wherein said data bits form a data pattern.

11. The method of claim 10, wherein said testing said analog circuit version is performed while applying a signal at said clock input.

12. The method of claim 11, wherein said testing said analog circuit version is performed while varying said clock input signal.

13. The method of claim 10 wherein said testing said analog circuit version is performed while varying said data pattern.

14. The method of claim 10, wherein said interconnecting logic blocks comprise Exclusive-Or gates, and wherein said testing said analog circuit version is performed while varying said data pattern using said Exclusive-Or gates.

15. The method of claim 10, wherein said interconnecting blocks comprise a plurality of logic paths, wherein each logic path is comprised of differing amounts of logic gates, and wherein said testing of said analog circuit portion is performed while alternately selecting from among said plurality of logic paths.

16. The method of claim 10, wherein at least one of said flip-flops is coupled to an equal number of pads through an equal number of output drivers, which may be enabled and disabled.

17. The method of claim 16, wherein said testing of said analog circuit portion is performed while enabling and disabling said output drivers.

18. The method of claim 1 wherein said analog circuit portion includes an RF circuit subportion.

19. The method of claim 1, wherein a number of gates in said emulation circuit is substantially equivalent to a number of gates in said digital circuit portion.

20. An integrated circuit having digital and analog circuit portions, said digital circuit portion comprising a digital noise emulation circuit, wherein said digital noise emulation circuit comprises:

a control block;

at least one array, which comprises at least one shift register; and

a plurality of pads.

21. The integrated circuit of claim 20, wherein each array comprises a plurality of flip-flops coupled to each other through interconnecting logic blocks.

22. The integrated circuit of claim 21, wherein said flip-flops and interconnecting logic blocks are coupled sequentially.

23. The integrated circuit of claim 22 wherein said control block comprises:

a plurality of configuration registers;

at least one input line;

a decoder block for selecting one of said configuration registers for updating from said at least one input line.

24. The integrated circuit of claim 23, wherein said interconnecting logic blocks comprise a plurality of logic paths, each path comprising a different amount of logic gates.

25. The integrated circuit of 24, wherein said plurality of logic paths are under control of one of said configuration registers.

26. The integrated circuit of claim 23, wherein said interconnecting logic blocks comprise an Exclusive-Or gate.

27. The integrated circuit of claim 26, wherein said exclusive-or gates receive at least one input from one of said configuration registers.

28. The integrated circuit of claim 23, wherein at least one flip-flops couples to an equal number of said plurality of pads.

29. The integrated circuit of claim 28, wherein said at least one flip-flops couples to an equal number of said plurality of pads though an equal number of output drivers.

30. The integrated circuit of claim 29, wherein said output drivers may be enabled and disabled by one of said configuration registers.

31. A method of designing an integrated circuit having digital and analog circuit portions, said digital and analog circuit portions each having defined functions, comprising:

providing an emulation circuit, which is capable of generating noise, and which comprises a plurality of logic elements;

affixing said emulation circuit on said integrated circuit;

providing a version of said analog circuit portion having at least some of the defined functions of said analog circuit portion;

affixing said analog circuit version on said integrated circuit;

testing said analog circuit version.

32. The method of claim 31 further comprising modifying said analog portion in response to said testing.

33. The method of claim 32 further compromising:

repeating said affixing emulation circuit step, said analog circuit portion providing step, said analog circuit portion version affixing step and said analog circuit portion version testing circuit step so that a version of said analog circuit portion having all of said defined functions of said analog circuit portion, with acceptable response to said noise effects under operating conditions is obtained.

34. The method of claim 31 further comprising reconnecting said logic elements to provide for said digital portion.

35. The method of claim 31, wherein said noise generated by said emulation circuit is substantially equivalent to said digital circuit portion.

36. An integrated circuit having digital and analog portions, designed by a process comprising:

providing an emulation circuit, which generates noise;

affixing said emulator circuit on a test substrate;

providing a version of said analog circuit portion having at least sone of said defined functions of said analog circuit portion;

affixing said analog circuit version on said test substrate; and

testing said analog circuit version.

37. The integrated circuit of claim 36, designed by a process further comprising modifying said analog portion in response to said testing step.

38. The integrated circuit of claim 37, designed by a process further compromising:

repeating said affixing emulation circuit step, said analog circuit portion providing step, said analog circuit portion version affixing step and said analog circuit portion version testing circuit step so that a version of said analog circuit portion having all of said defined functions of said analog circuit portion, with acceptable response to said noise effects under operating conditions is obtained.

39. The integrated circuit of claim 36, designed by a process further comprising:

providing a version of said digital circuit portion having all of said defined functions of said digital circuit portion; and

affixing said digital circuit portion version to an integrated circuit including said version of said analog circuit portion having all of said defined functions of said analog circuit portion, with acceptable response to said noise effects under operating conditions.

40. The integrated circuit of claim 36 wherein said emulation circuit has at least one array comprising at least one shift register.

41. The integrated circuit of claim 40, wherein said shift register comprises:

a plurality of flip-flops, each having a clock input for receiving a clock input signal, and each storing a data bit; and

a plurality of interconnecting logic blocks, wherein said plurality of flip-flops couple to each other through said plurality of interconnecting logic blocks sequentially, and wherein said data bits form a data pattern.

42. The integrated circuit of claim 36 wherein said analog circuit portion includes an RF circuit subportion.

43. The integrated circuit of claim 36, wherein a number of gates in said emulation circuit is substantially equivalent to a number of gates in said digital circuit portion.